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QUERY CONTROL FORM		RTIS USE ONLY
Application No. 10/085,023	Prepared by J. Robbins	Tracking Number 05873924
Examiner-GAU Flynn-2826	Date 1-27-04	Week Date 12-8-03
	No. of queries 01	IFW

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JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION

a. Page Missing
b. Text Continuity
c. Holes through Data
d. Other Missing Text
e. Illegible Text
f. Duplicate Text
g. Brief Description
h. Sequence Listing
i. Appendix
j. Amendments
k. Other

CLAIMS

a. Claim(s) Missing
b. Improper Dependency
c. Duplicate Numbers
d. Incorrect Numbering
e. Index Disagrees
f. Punctuation
g. Amendments
h. Bracketing
i. Missing Text
j. Duplicate Text
k. Other

MESSAGE Patent claim 6 (original claim 10), line 4 is illegible - Claims dated 9-23-2003.

Thank You

initials

RESPONSE Attorney faxed clear copy of amendment pages.

initials

E-5 (Rev. 10/01/02)

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FACSIMILE

Date:	February 11, 2004
To:	Examiner Fairchild Patent and Trademark Office
Re:	**Response to Office Action dated September 23, 2003** U.S. Patent Application Serial No.: **10/085,023** By: **Hideo KURIHARA et al.** Your Reference: **F0786P-PCT-US** Our Reference: **020137**
Fax Number:	703-305-4372
Number of Pages	16 (including cover sheet)
From:	Thomas E. Brown TB

To Whom It May Concern:

Attached to this Fax is a copy of the Response under 37 C.F.R. §1.116; Petition for Extension of Time and Date Stamped Post Card which were filed on September 23, 2003.

PLEASE ACKNOWLEDGE SAFE AND CLEAR RECEIPT OF ALL PAGES BEING SENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **KURIHARA, Hideo et al.**

Group Art Unit: **2826**

Serial No.: **10/085,023**

Examiner: **Scott R. Wilson**

Filed: **March 1, 2002**

P.T.O. Confirmation No.: 8810

For. **TWO-BIT SEMICONDUCTOR MEMORY WITH ENHANCED CARRIER TRAPPING (AS AMENDED)**

PETITION FOR EXTENSION OF TIME

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Date: September 23, 2003

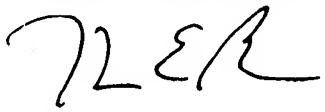
Sir:

Applicants petition the Commissioner for Patents to extend the time for response to the Office Action dated May 23, 2003 for one month from August 23, 2003 to September 23, 2003.

Attached please find a check in the amount of $110.00 to cover the cost of the extension for a large entity. In the event that any additional fees are due in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



Thomas E. Brown
Attorney for Applicant
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Customer Number
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **KURIHARA, Hideo et al.**

Serial No.: **10/085,023**

Group Art Unit: **2826**

Filed: **March 1, 2002**

Examiner: **Scott R. Wilson**

P.T.O. Confirmation No.: 8810

For: **TWO-BIT SEMICONDUCTOR MEMORY WITH ENHANCED CARRIER TRAPPING (AS AMENDED)**

AMENDMENT UNDER 37 C.F.R. §1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

September 23, 2003

Sir:

In response to the Office Action dated **May 23, 2003**, extended to **September 23, 2003** by a one-month Petition for Extension of Time, please amend the above-identified application as follows:

Amendments to Specification are reflected on page 2 of this paper.

Amendments to Claims are reflected in the listing of claims which begins on page 3 of this paper.

Amendments to the Drawings begin on page 9 of this paper and include an replacement sheet of drawings.

Remarks/Arguments begin on page 10 of this paper.

An Appendix including amended drawing figures is attached following page 13 of this paper.

Amendments to the Specification:

In the Title:

Replace the title in its entirety to read as follows:

TWO-BIT SEMICONDUCTOR MEMORY WITH ENHANCED CARRIER TRAPPING

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A semiconductor memory comprising:

a pair of diffused layers formed in a surface area of a semiconductor substrate; and

a gate electrode formed on a gate insulating film on the semiconductor substrate between said pair of diffused layers, so that carriers are trapped in the gate insulating film by applying a predetermined voltage to said gate electrode, thereby 2-bit information is capable of being recorded, and wherein

the gate insulating film is formed higher in carrier trap characteristic at positions near said pair of diffused layers than in a remaining area.

Claim 2 (Original): A semiconductor memory according to claim 1, wherein a charge trap film higher in carrier trap characteristic than said gate insulating film is formed in said gate insulating film at the positions near said pair of diffused layers.

Claim 3 (Original): A semiconductor memory according to claim 2, wherein said gate insulating film is formed thinner at the positions near said pair of diffused layers than in the remaining area.

Claim 4 (Original): A semiconductor memory according to claim 1, wherein said gate insulating film is formed smaller in film thickness in electrical capacitance conversion at the positions near said pair of diffused layers than in the remaining area.

Claim 5 (Original): A semiconductor memory according to claim 2, wherein another charge trap film is formed on said gate insulating film, and said gate electrode is formed on said other charge trap film on said gate insulating film.

Claim 6 (Withdrawn): A method of manufacture of a semiconductor memory, comprising:

a first step for sequentially forming first and second insulating films on a semiconductor substrate;

a second step for selectively removing and patterning said first and second insulating films;

a third step for forming a third insulating film on said semiconductor substrate in a predetermined range from said exposed semiconductor substrate to a layer below said second insulating film;

a fourth step for introducing impurities into said semiconductor substrate by utilizing said second insulating film as a mask, thereby forming a pair of independent diffused layers in a surface area of said semiconductor substrate at two sides of said second insulating film;

a fifth step for leaving said third insulating film formed in the predetermined range below said second insulating layer, and removing said third insulating film in a remaining area to expose

said semiconductor substrate;

a sixth step for thermally oxidizing said exposed semiconductor substrate to form an element isolation film;

a seventh step for removing said first and second insulating films to expose said underlying semiconductor substrate and third insulating film, and causing said third insulating film to function as a charge trap film;

a eighth step for thermally oxidizing the exposed surface of said semiconductor substrate to form a fourth insulating film, and covering upper and lower surfaces of said charge trap film with the fourth insulating film;

a ninth step for forming a conductive film on said fourth insulating film; and

a tenth step of patterning said conductive film into a gate electrode shape.

Claim 7 (Withdrawn): A method of manufacture of a semiconductor memory according to claim 6, further comprising, between said second and third steps, the eleventh step for removing said first insulating film by a predetermined amount in a direction of pattern width to make the pattern width of said first insulating film smaller than the pattern width of said second insulating film, and wherein

in the third step, said third insulating film is formed on said exposed semiconductor substrate and on said semiconductor substrate within a range of said predetermined amount.

Claim 8 (Withdrawn): A method of manufacture of a semiconductor memory according to claim 6, further comprising, between said eighth and ninth steps, the twelfth step for forming a fifth insulating film on said fourth insulating film, and wherein

in the ninth step, said conductive film is formed on said fifth insulating film on said fourth insulating film.

Claim 9 (Withdrawn): A method of manufacture of a semiconductor memory, comprising the steps of:

forming a first insulating film on a semiconductor substrate;

selectively removing said first insulating film to expose said underlying semiconductor substrate;

introducing impurities into said exposed semiconductor substrate by using said first insulating film as a mask;

forming a pair of independent impurity diffused layers in a surface area of said semiconductor substrate at two sides of said first insulating film;

forming a second insulating film so as to cover said impurity diffused layers and said first insulating film;

removing said second insulating film on said first insulating film to expose said first insulating film;

removing said first insulating film to expose said underlying semiconductor substrate, thereby

causing this area to function as an active element area;

forming a third insulating film on said semiconductor substrate in said active element area;

forming a fourth insulating film on said third insulating film;

forming a fifth insulating film so as to cover said fourth and second insulating films;

removing said fifth insulating film so as to remain only on two sides of said active element area, thereby forming a side wall of said fifth insulating film on a side wall of said second insulating film and exposing said semiconductor substrate in said active element area;

forming a sixth insulating film on said exposed semiconductor substrate;

removing said side wall to expose said underlying fourth insulating film of said side wall, thereby causing said fourth insulating film to function as a charge trap film;

forming a seventh insulating film on said charge trap film; and

forming a conductive film so as to cover said sixth and seventh insulating films.

Claim 10 (New): A semiconductor memory comprising:

a pair of diffused layers formed in a surface area of a semiconductor substrate; and

a gate electrode formed on a gate insulating film on the semiconductor substrate between said pair of diffused layers, so that carriers are trapped in the gate insulating film by applying a predetermined voltage to said gate electrode, and wherein

the gate insulating film is formed higher in carrier trap characteristic at positions near said pair of diffused layers than in a remaining area,

a charge trap film higher in carrier trap characteristic than said gate insulating film is formed in said gate insulating film at the positions near said pair of diffused layers, and

another charge trap film is formed on said gate insulating film, and said gate electrode is formed on said other charge trap film on said gate insulating film.

Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 8. This sheet, which includes Fig.8, replaces the original sheet including Fig. 8. Amended Fig. 8 has been labeled as prior art as suggested by the Examiner on page 2 of the outstanding Office Action.

REMARKS

Claims 1 - 9 are pending in this application, of which claims 6 - 9 have been withdrawn from consideration. By this Amendment, claim 1 has been amended and new claim 10 has been added. The applicants respectfully submit that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated **May 23, 2003**.

Allowable Subject Matter:

Applicants gratefully acknowledge the indication on page 4 of the Action, that claim 5 would be allowable if rewritten in independent form to include all of the features of its base claim 1 and intervening claim 2.

It is respectfully submitted that newly added claim 10 includes the allowable features of claim 5 and its base claim 1 and intervening claim 2. Therefore, it is submitted that claim 10 is allowable.

In the Drawings

The Examiner has required, that Fig. 8 be labeled as prior art. As such, attached herewith is a replacement sheet of drawings including Fig. 8 which has been labeled prior art. Accordingly, withdrawal of this objection to the drawings is respectfully solicited.

In the Specification

The Examiner has required a new, more descriptive title. Accordingly, pursuant to the Examiner's suggestion on page 2 of the outstanding Office Action, the title has been amended to read:

TWO-BIT SEMICONDUCTOR MEMORY WITH ENHANCED CARRIER TRAPPING

Accordingly, withdrawal of this objection to the title is respectfully solicited.

As to the Merits:

As to the merits of this case, the Examiner sets forth the following rejections:

1) claims 1 and 2 stand rejected under 35 U.S.C. §102(b) as being anticipated by Eitan (U.S. Patent No. 5,768,192); and

2) claims 1 - 4 stand rejected under 35 U.S.C. §102(b) as being anticipated by Tomioka (U.S. Patent No. 5,796,140).

Each of these rejections are respectfully traversed.

In Tomioka, as indicated in Fig. 7 and its description, a memory is on the condition that it has a structure of a floating gate. That is, the memory forms a floating gate which consists of 104,

114, and 115 (each of them is poly-silicon) in the Drawing and also it consists of a control gate 117 formed on an insulating film 116. Although, it is indicated therein that electrons are injected in 114 of the floating gate through a tunneling oxynitride film near the source/drain, electrons are not trapped in only 114 since the floating gate is a conductor and electrons spread to the entire floating gate.

Whereas, the memory of the present invention does not have a floating gate, and it traps electrons in (the high carrier trap characteristic part of) the gate insulating film.

Accordingly, Tomioka is completely different from the present invention.

In Eitan, as shown in Fig. 8B and its description, it just discloses the prior art described in the present invention as the memory structure. That is, region 68 in Fig. 8B is only indicated to describe the state that charges are trapped in a charge trap layer.

Accordingly, Tomioka and Eitan each fail to disclose or suggest the feature of the present invention that the carrier trap characteristic of the charge trap layer near the source and the drain is higher than other parts.

If, for any reason, it is felt that this application is not now in condition for allowance, the

Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

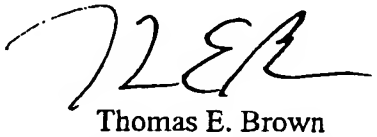

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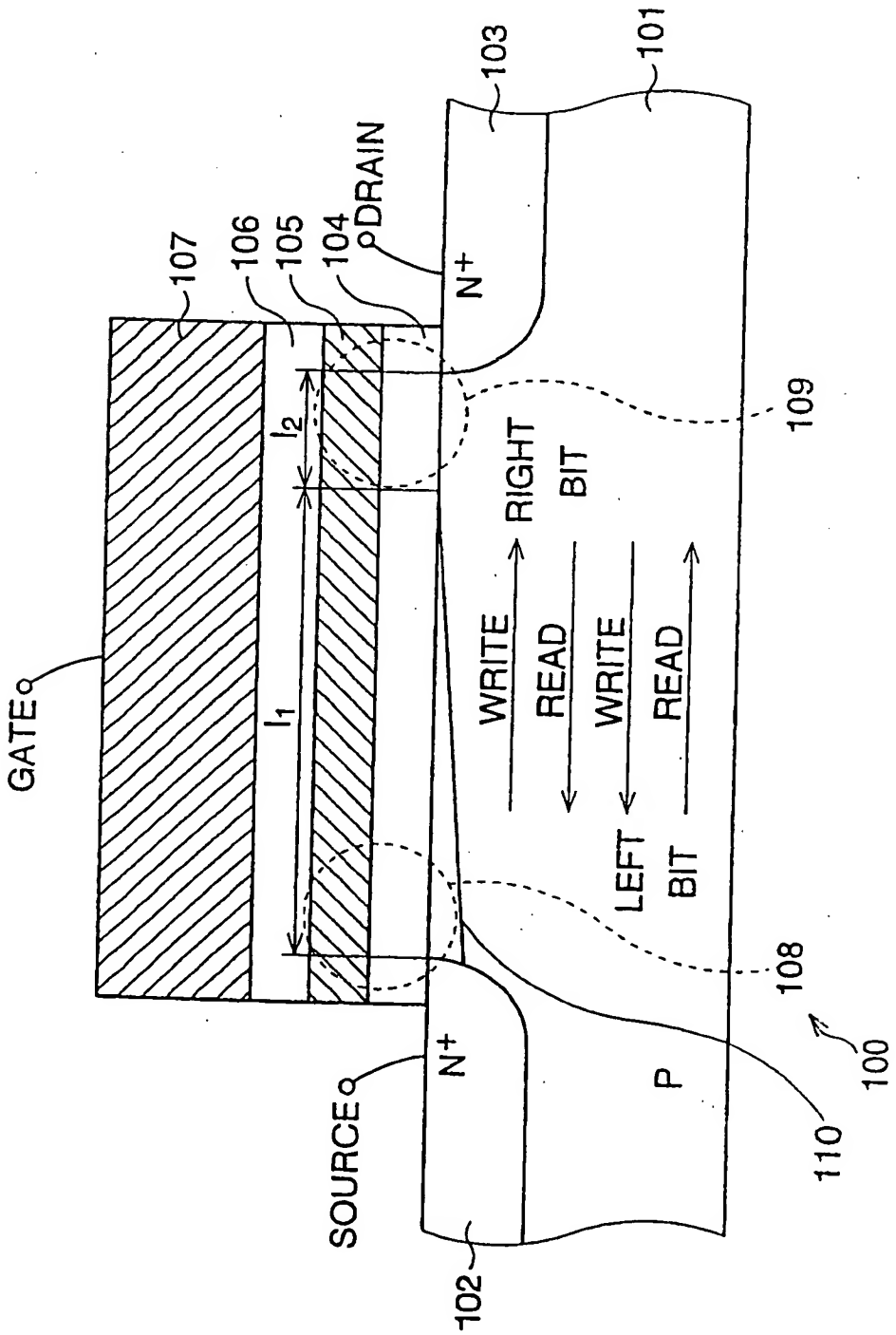
FIG. 8
PRIOR ART



CARD NO: 05473

U.S. Patent Application
Serial No: 10/085,023
Patent Number:
Applicant(s): KURIHARA, Hideo et al.

Docket No: 020137
Filed: 03/01/02
Issued:

Papers filed herewith on: 09/23/03

Fees: $ 110.00 Amendment
Req. for Ext. of Time

Other: Replacment Sheet of Drawings for Figure 8

COMMISSIONER OF PATENTS

Receipt is heraby acknowledged of the papers filed as indicated in connection with the above-identified case.

TEB/KAL